

این دیتاشیت توسط توکل الکترونیک تهیه و ارائه شده است.
جهت مشاهده قیمت، موجودی و ثبت سفارش این قطعه به وبسایت توکل الکترونیک مراجعه فرمایید.



مشاهده قیمت و خرید

برای خرید و مشاهده سایر محصولات کلیک کنید



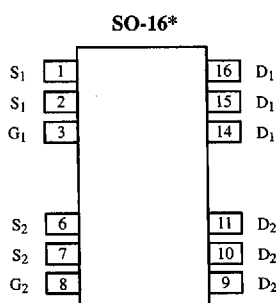
TEMIC
Semiconductors

Si9940DY

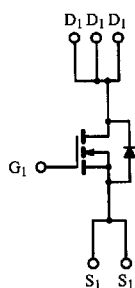
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

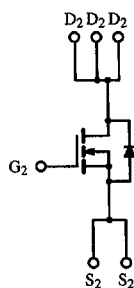
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.05 @ $V_{GS} = 10$ V	± 5.3
	0.07 @ $V_{GS} = 4.5$ V	± 4.5



*Conforms to standard SO-16 dimensions



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	50	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 5.3	A
		± 4.2	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	2.5	W
Maximum Power Dissipation ^a	P_D	2.5	
		1.6	
Operating Junction and Storage Temperature Range	T_J, T_{sig}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1211. A SPICE Model data sheet is available for this product (FaxBack document #5106).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

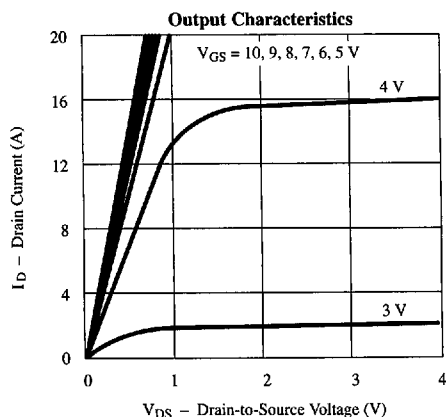
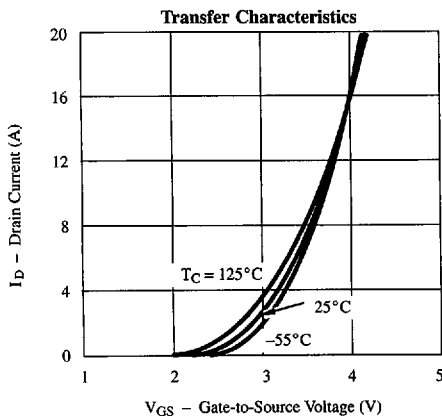
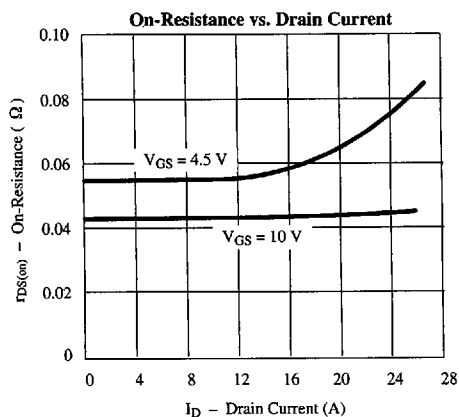
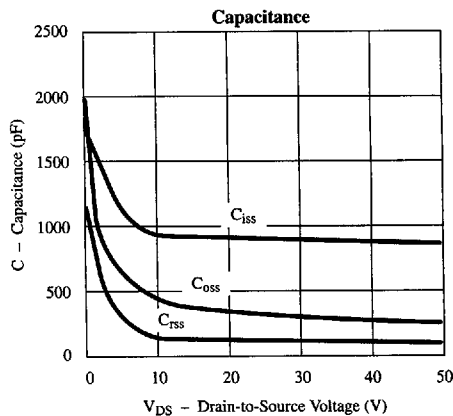
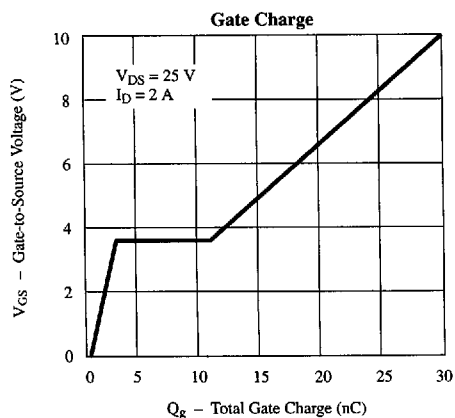
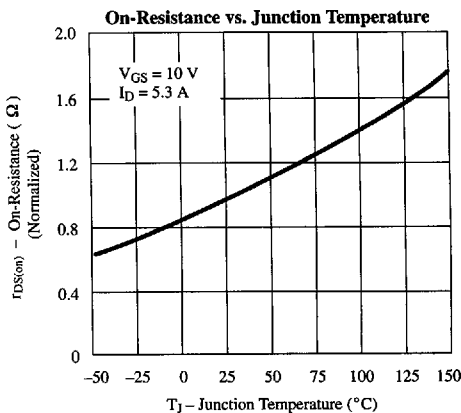
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\ \text{V}, V_{GS} = 0\ \text{V}$			2	μA
		$V_{DS} = 40\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 5.3\ \text{A}$		0.042	0.05	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 4.5\ \text{A}$		0.055	0.07	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 5.3\ \text{A}$		11		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.5\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 25\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 2\ \text{A}$		30	50	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			9.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25\ \text{V}, R_L = 25\ \Omega$ $I_D \approx 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		17	40	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	t_f			55	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		130		

Notes

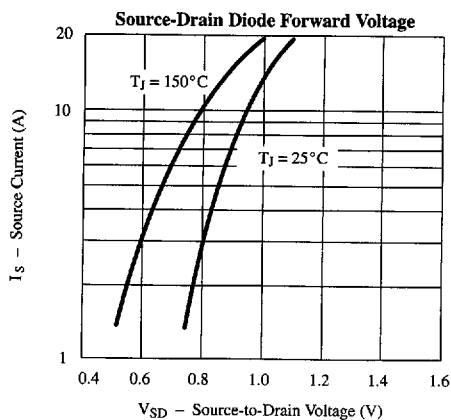
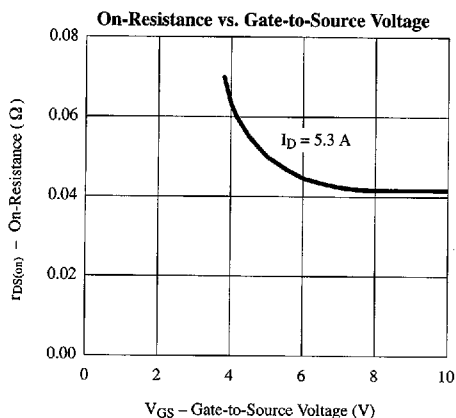
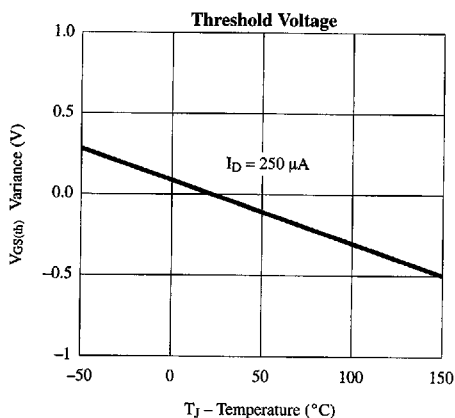
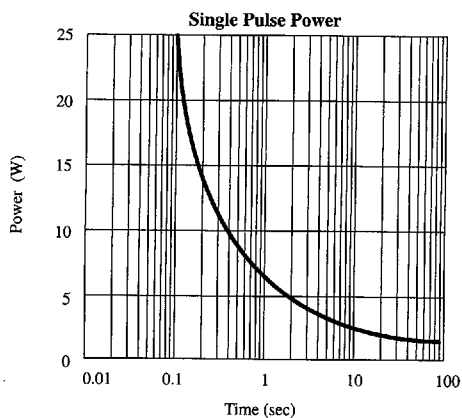
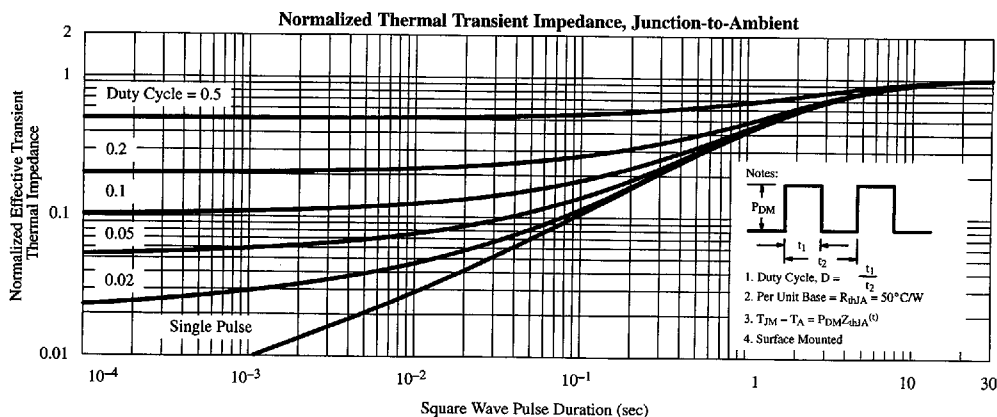
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

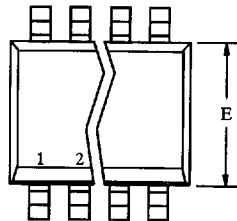
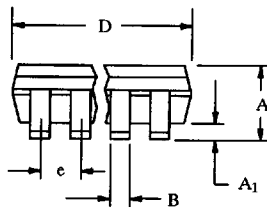
Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)



SO Package (Y Suffix), 8-16 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-14	8.35	8.95	0.329	0.352
D-16	9.60	10.20	0.378	0.402
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

