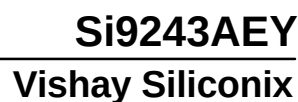




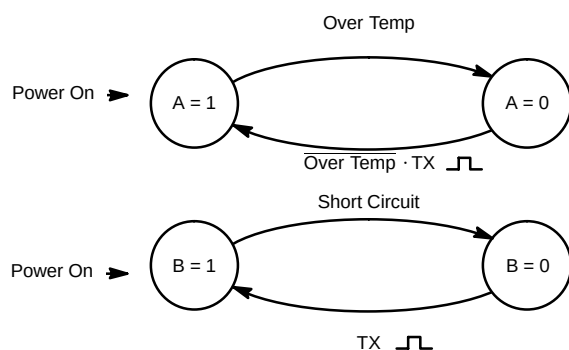
مشاهده قیمت و خرید

برای خرید و مشاهده سایر محصولات کلیک کنید





OUTPUT TABLE AND STATE DIAGRAMS



Note: Over Temp is an internal condition, not meant to be a logic signal.

INPUTS		STATE VARIABLE		OUTPUT TABLE			Comments
TX	L	A	B	K	RX _K	RX _L	
0	0	1	1	0	0	0	Over Temp Short Circuit
1	1	1	1	1	1	1	
0	1	1	1	0	0	1	
1	0	1	1	1	1	0	
X	L	0	1	HiZ	K	L	
0	L	1	0	HiZ	K	L	
1	1	1	1	1	1	1	Receive Mode
1	0	1	1	0	0	0	

X = "1" or "0"
HiZ = High Impedance State

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to Ground
 Voltage On V_{BAT} -24 V to 45 V
 Voltage K, L -16 V to (V_{BAT} + 1 V)
 Voltage Difference V_(VBAT, K, L) 55 V
 Voltage On Any Pin (Except V_{BAT}, K, L)
 or Max. Current -0.3 V to (V_{DD} + 0.3 V) or 10 mA

Voltage on V_{DD} 7 V
 K Pin Only, Short Circuit Duration (to V_{BAT} or GND) Continuous
 Operating Temperature (T_A) -40 to 125°C
 Junction and Storage Temperature -55 to 150°C
 Thermal Resistance Θ_{JA} 125°C/W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Voltage Referenced to Ground
 V_{DD} 4.5 V to 5.5 V
 V_{BAT} 6 V to 36 V

K, L 6 V to 36 V
 Digital Inputs 0 to V_{DD}

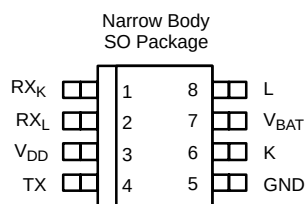


SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 4.5$ to 5.5 V $V_{BAT} = 6$ to 36 V		Temp ^a	Limits −40 to 125°C			Unit
					Min ^b	Typ ^c	Max ^b	
Transmitter and Logic Levels								
TX Input Low Voltage	V_{ILT}			Full			1.5	V
TX Input High Voltage	V_{IHT}			Full	3.5			
TX Input Capacitance ^d	C_{INT}			Full			10	pF
TX Input Pull-up Resistance	R_{TX}	$V_{DD} = 5.5$ V, TX = 1.5 V, 3.5 V		Full	10	20	40	kΩ
K Transmit								
K Output Low Voltage	V_{OLK}	$R_L = 510\ \Omega \pm 5\%$, $V_{BAT} = 6$ to 18 V		Full			$0.2\ V_{BAT}$	V
		$R_L = 1\ k\Omega \pm 5\%$, $V_{BAT} = 16$ to 36 V		Full			$0.2\ V_{BAT}$	
		$R_L = 510\ \Omega \pm 5\%$, $V_{BAT} = 4.5$ V		Full			1.2	
K Output High Voltage	V_{OHK}	$R_L = 510\ \Omega \pm 5\%$, $V_{BAT} = 4.5$ to 18 V		Full	$0.95\ V_{BAT}$			
		$R_L = 1\ k\Omega \pm 5\%$, $V_{BAT} = 16$ to 36 V		Full	$0.95\ V_{BAT}$			
K Rise, Fall Times	t_r, t_f	See Test Circuit		Full			9.6	μs
K Output Sink Resistance	R_{Si}	TX = 0 V		Full			110	Ω
K Output Capacitance ^d	C_O			Full			20	pF
Receiver								
L and K Input High Voltage	V_{IH}			Full	$0.65\ V_{BAT}$			V
L and K Input Hysteresis ^{c, d}	V_{HYS}			Full		$0.05\ V_{BAT}$		
L and K Input Currents	I_{IH}	TX = 4 V	$V_{IH} = V_{BAT}$	Full			20	μA
RX _L and RX _K Output Low Voltage	V_{OLR}		$V_{ILK}, V_{ILL} = 0.35\ V_{BAT}$ $I_{OLR} = 1$ mA	Full			0.4	V
RX _L and RX _K Pull-up Resistance	R_{RX}			Full	5		20	kΩ
RX _K Turn On Delay	$t_{d(on)}$	$R_L = 510\ \Omega \pm 5\%$, $V_{BAT} = 6$ to 18 V $C_L = 10$ nF, See Test Circuit		Full		3	10	μs
		$R_L = 1\ k\Omega \pm 5\%$, $V_{BAT} = 16$ to 36 V $C_L = 4.7$ nF, See Test Circuit		Full		3	10	
RX _K Turn Off Delay	$t_{d(off)}$	$R_L = 510\ \Omega \pm 5\%$, $V_{BAT} = 6$ to 18 V $C_L = 10$ nF, See Test Circuit		Full		3	10	
		$R_L = 1\ k\Omega \pm 5\%$, $V_{BAT} = 16$ to 36 V $C_L = 4.7$ nF, See Test Circuit		Full		3	10	
Supplies								
Bat Supply Current On	$I_{BAT(on)}$	TX = 0 V, $V_{BAT} \leq 16$ V		Full		1.2	3	mA
Bat Supply Current Off	$I_{BAT(off)}$	$V_{IHT} \leq V_{TX}$, $V_{IHK} \leq V_K$, $V_{IHL} \leq V_L$, $V_{BAT} \leq 12$ V		Full		120	220	μA
Bat Supply Current Standby	$I_{BAT(SB)}$	$V_{DD} \leq 0.5$ V, $V_{BAT} \leq 12$ V		Full		< 1	10	
Logic Supply Current On	$I_{DD(on)}$	$V_{DD} \leq 5.5$ V, TX = 0 V		Full		1.4	2.3	mA
Logic Supply Current Off	$I_{DD(off)}$	$V_{IHT} \leq V_{TX}$, $V_{IHK} \leq V_K$, $V_{IHL} \leq V_L$, $V_{BAT} \leq 12$ V		Full			10	μA
Miscellaneous								
TX Transmit Baud Rate	BR_T	$R_L = 510\ \Omega$, $C_L = 10$ nF		Full	10.4			kBaud
RX _L and RX _K Receive Baud Rate ^c	BR_R	$6\ V < V_{BAT} < 16\ V$, $C_{RX} = 20$ pF		Full		200		
Transmission Frequency	f_{K-RXK}	$6\ V < V_{BAT} < 16\ V$, $R_K = 510\ \Omega$, $C_K \leq 1.3$ nF		Full	50	200		kHz
TX Minimum Pulse Width ^{d, e}	t_{TX}			Full	1			μs
Over Temperature Shutdown ^d	T_{SHUT}	Temperature Rising			160	180		°C
Temperature Shutdown Hysteresis ^c	T_{HYST}					30		

Notes

- Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- Minimum pulse width to reset a fault condition.

PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Temperature Range
Si9243AEY	−40 to 125°C

PIN DESCRIPTION

Pin Number	Symbol	Description
1	RX _K	K Receiver, Output
2	RX _L	L Receiver, Output
3	V _{DD}	Positive Power Supply
4	TX	Transmit, Input
5	GND	Ground Connection
6	K	K Transmit/Receive, Bidirectional
7	V _{BAT}	Battery Power Supply
8	L	L Transmit, Input

FUNCTIONAL DESCRIPTION

The Si9243AEY can be either in transmit or receive mode and it contains over temperature, and short circuit V_{BAT} fault detection circuits.

The voltage on the K and L pins are internally compared to V_{BAT/2}. If the voltage on the K or L pin is less than V_{BAT/2} then RX_K or RX_L output will be “low.” If the voltage on the K or L pin is greater than V_{BAT/2} then RX_K or RX_L output will be “high.”

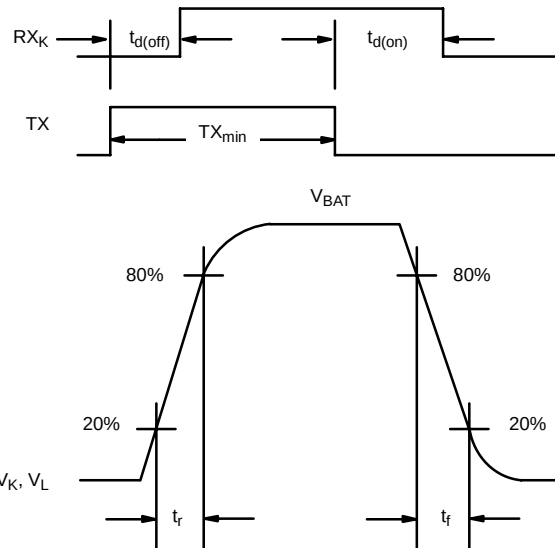
In order to be in transmit mode, TX must be set “low.” The TX signal is then internally inverted and turns the MOSFET on, causing the K pin to be “low.” In transmit mode, the processor

monitors the RX_K and TX. When the two mirror each other there is no fault. In the event of over temperature, or short circuit to V_{BAT}, the Si9243AEY will turn off the K output to protect the IC. The K pin will stay in high impedance and RX_K will follow the K pin. The fault will be reset when TX is toggled high. RX_K, RX_L and TX pins have internal pull up resistor to V_{DD} while K and L pins have internal pull down resistors. When any one of the TX, V_{BAT} or GND pins is open the K output is off.

When the TX pin is set “high” the Si9243AEY is in receive mode and the internal MOSFET is turned off. RX_L and RX_K outputs will follow L and K inputs respectively.

The schematic diagram illustrates the internal structure of the Si9243AEY transceiver. The IC is represented by a large rectangle with pins for V_{DD} , V_{BAT} , RX_L , RX_K , TX , L , K , and GND . Inside the IC, three input buffers are shown: two inverters for RX_L and RX_K , and a NAND-inverter for TX . A voltmeter 'V' is connected across the inputs of the first two inverters. The output of the first inverter is connected to pin L . The output of the second inverter is connected to pin K . The output of the NAND-inverter is connected to a transistor, which is in turn connected to pin K . A pull-up resistor is connected to pin K and V_{BAT} . A capacitor C_L is connected to pin K and GND . A diode is connected between the output of the NAND-inverter and the transistor. A resistor is connected between the output of the NAND-inverter and GND . The diagram also shows external components: R_L and R_K are resistors connected to pins L and K respectively, and C_L is a capacitor connected to pin K and GND . The values of these components are specified as $R_L = 510 \Omega$, $C_L = 1$, and $R_K = 1 \text{ k}\Omega$, $C_L = 4$.

$$R_L = 510 \, \Omega, C_L = 10 \, \text{nF}, V_{\text{BAT}} = 6 \, \text{V to } 18 \, \text{V}$$

$$R_L = 1 \, \text{k}\Omega, C_L = 4.7 \, \text{nF}, V_{\text{BAT}} = 16 \, \text{V to } 36 \, \text{V}$$


The diagram illustrates the electrical connection between an ECU (Electronic Control Unit) and a Diagnostic Tester. The ECU is shown as a large box containing a Microcontroller, a Si9243AEY chip, and various passive components. The Microcontroller has three I/O pins. The Si9243AEY chip is powered by V_{BAT} and V_{DD} (50V) and includes a voltage divider, a voltage source, and a transistor. The Diagnostic Tester is connected to the ECU's L-Line and K-Line, which are part of a CAN bus system. The tester includes a voltage source V_B, a 510 Ω resistor, and a 0.4 Ω resistor.

ECU = Electronic Control Unit