

این دیتاشیت توسط توکل الکترونیک تهیه و ارائه شده است.
جهت مشاهده قیمت، موجودی و ثبت سفارش این قطعه به وبسایت توکل الکترونیک مراجعه فرمایید.



مشاهده قیمت و خرید
برای خرید و مشاهده سایر محصولات کلیک کنید



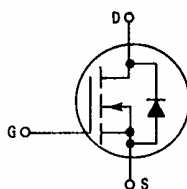
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTH40N08
MTH40N10
MTH40N05
MTH40N06

TMOS POWER FETs
and AMPERES
 $r_{DS(on)} = 0.04 \text{ OHM}$
80 and 100 VOLTS
 $r_{DS(on)} = 0.028 \text{ OHM}$
50 and 60 VOLTS



CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH				Unit
		40N05	40N06	40N08	40N10	
Drain-Source Voltage	V _{DSS}	50	60	80	100	V _{dc}
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	50	60	80	100	V _{dc}
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40				V _{dc} V _{pk}
Drain Current Continuous Pulsed	I _D I _{DM}	40 140		40 120		A _{dc}
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T _J , T _{sta}	− 65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.833 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (VGS = 0, ID = 0.25 mA) MTH40N05 MTH40N06 MTH40N08 MTH40N10	V(BR)DSS	50 60 80 100	— — — —	Vdc	
Zero Gate Voltage Drain Current (VDS = Rated VDS, VGS = 0) (VDS = Rated VDS, VGS = 0, TJ = 125°C)	IDSS	— —	10 100	μAdc	
Gate-Body Leakage Current, Forward (VGSF = 20 Vdc, VDS = 0)	IGSSF	—	500	nAdc	
Gate Body Leakage Current, Reverse (VGSR = 20 Vdc, VDS = 0)	IGSSR	—	500	nAdc	
ON CHARACTERISTICS					
Gate Threshold VqIage (VDS = VGS, ID = 1 mA) TJ = 100°C	VGS(th)	2 1.5	4.5 4	Vdc	
Static Drain-Source On-Resistance (VGS = 10 Vdc, ID = 20 Adc) MTH40N05/06 MTH40N08/10	rDS(on)	— —	0.028 0.04	Ohm	
Drain-Source On-Voltage (VGS = 10 V) (ID = 40 Adc) (ID = 20 Adc, TJ = 100°C) (ID = 40 Adc) (ID = 20 Adc, TC 100°C) MTH40N05/06 MTH40N05/06 MTH40N08/10 MTH40N08/10	VDS(on)	— — — —	1.4 1.12 2 1.6	Vdc	
Forward Transconductance (VDS = 15 V, ID = 20 A)	gFS	10	—	mhos	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(VDS = 25 V, VGS = 0, f = 1 MHz) See Figure 8	Ciss	—	5000	pF
Output Capacitance		Coss	—	2500	
Reverse Transfer Capacitance		Crss	—	1000	
SWITCHING CHARACTERISTICS (TJ = 100°C)					
Turn-On Delay Time	(VDD = 25 V, ID = 0.5 Rated ID Rgen = 50 ohms) See Figure 16	td(on)	—	100	ns
Rise Time		tr	—	330	
Turn-Off Delay Time		td(off)	—	330	
Fall Time		tf	—	360	
Total Gate Charge	(VDS = 0.8 Rated VDS, ID = Rated ID, VGS = 10 Vdc) See Figure 15	Og	105 (Typ)	120	nC
Gate-Source Charge		Qgs	74 (Typ)	—	
Gate-Drain Charge		Qgd	31 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(IS = Rated ID, VGS = 0)	VSD	2.2 (Typ)	3	Vdc
Forward Turn-On Time		ton	Limited by stray inductance		
Reverse Recovery Time		trr	75 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	Ld	4 (Typ) 5 (Typ)	— —	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	Ls	10 (Typ)	—		

TYPICAL CHARACTERISTICS

MTH40N05, MTH40N06

FIGURE 1 — ON-REGION CHARACTERISTICS

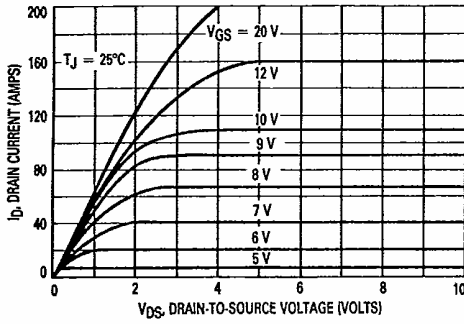


FIGURE 3 — TRANSFER CHARACTERISTICS

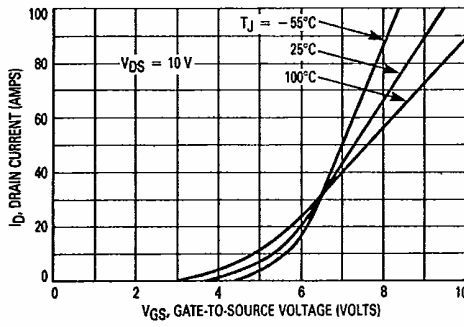
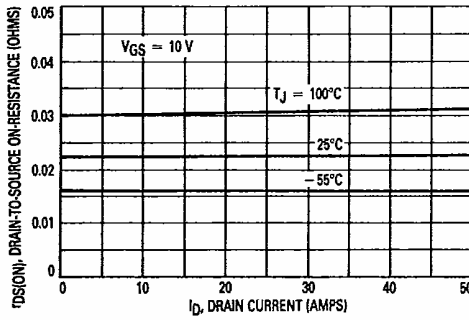


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTH40N08, MTH40N10

FIGURE 2 — ON-REGION CHARACTERISTICS

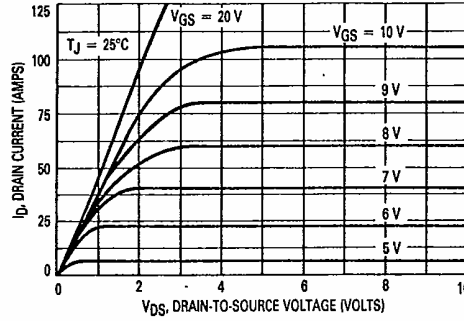


FIGURE 4 — TRANSFER CHARACTERISTICS

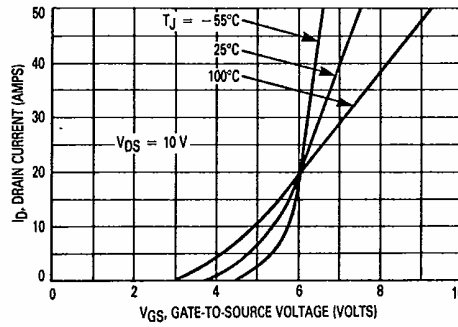
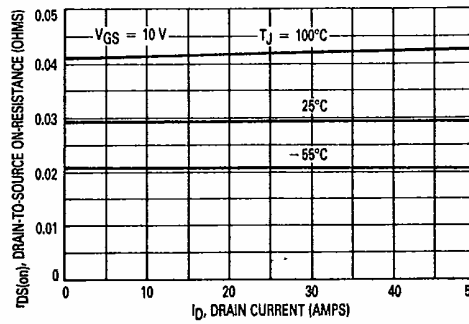


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

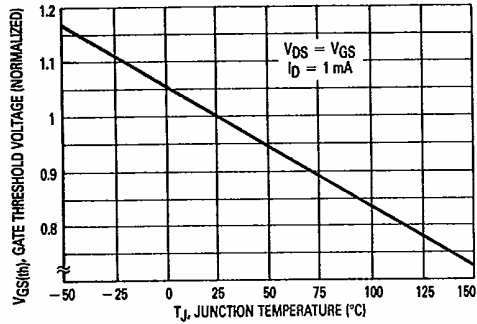


FIGURE 8 — CAPACITANCE VARIATION

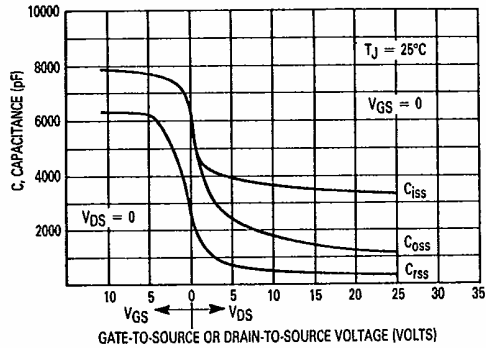


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

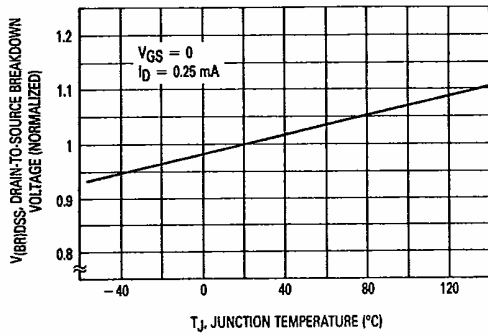


FIGURE 10 — ON-RESISTANCE VARIATION WITH TEMPERATURE

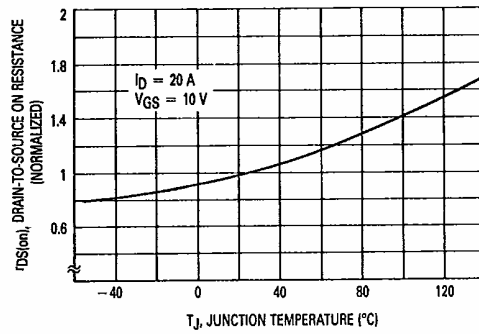
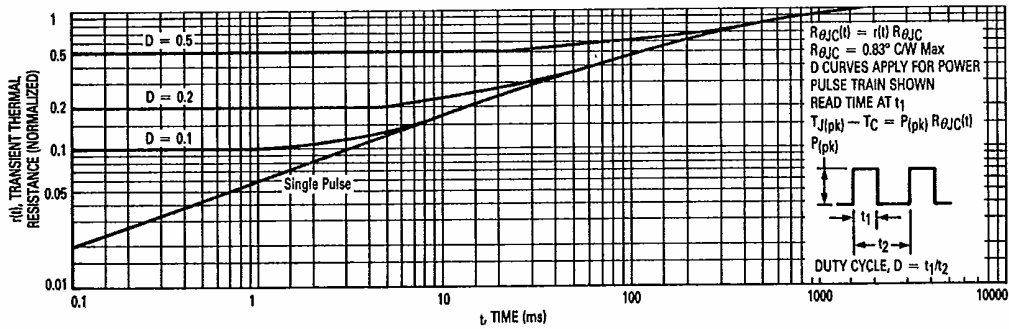


FIGURE 11 — THERMAL RESPONSE



MTH40N08, 10, 05, 06

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

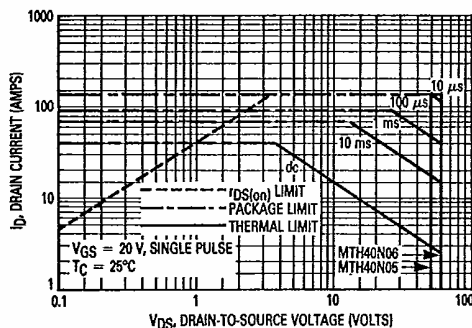
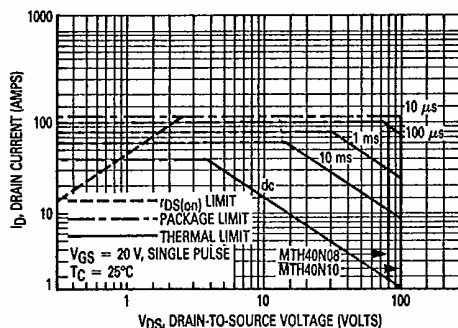


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(max) - T_C}{R_{\theta JC}}$$

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

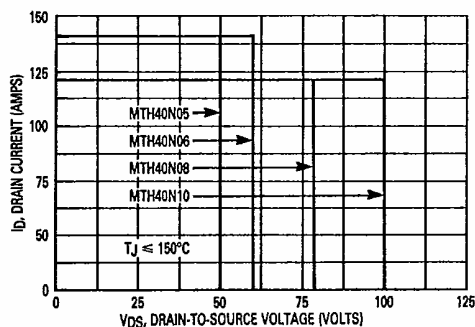


FIGURE 15 — STORED CHARGE versus GATE-TO-SOURCE VOLTAGE

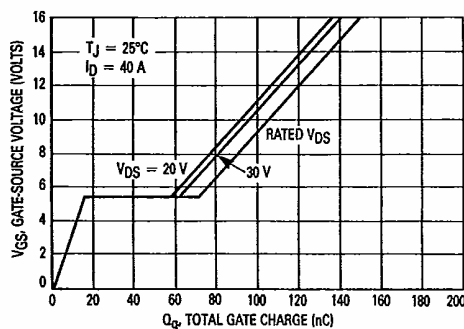


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE

