

این دیتاشیت توسط توکل الکترونیک تهیه و ارائه شده است.

جهت مشاهده قیمت، موجودی و ثبت سفارش این قطعه به وبسایت توکل الکترونیک مراجعه فرمایید.



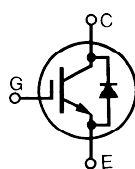
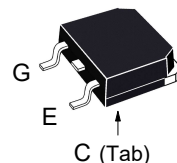
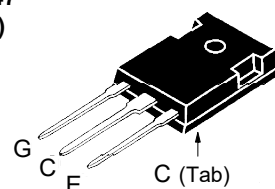
مشاهده قیمت و خرید

برای خرید و مشاهده سایر محصولات کلیک کنید



IXYS

Not for New Design

High Voltage, High Gain
BIMOSFET™ Monolithic
Bipolar MOS TransistorIXBT12N300
IXBH12N300 $V_{CES} = 3000V$ $I_{C110} = 12A$ $V_{CE(sat)} \leq 3.2V$ TO-268
(IXBT)TO-247
(IXBH)G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_C = 25^\circ C$ to $150^\circ C$	3000	V
V_{GGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	30	A
I_{C110}	$T_C = 110^\circ C$	12	A
I_{CM}	$T_C = 25^\circ C$, 1ms	100	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 30\Omega$ Clamped Inductive Load	$I_{CM} = 98$ 1500	A V
P_C	$T_C = 25^\circ C$	160	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-247)	1.13/10	Nm/lb.in.
Weight	TO-268	4	g
	TO-247	6	g

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			25 μA 1 mA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 12A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$	2.8		3.2 V
		3.5		V

Features

- High Blocking Voltage
- International Standard Packages
- Anti-Parallel Diode
- Low Conduction Losses

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications:

- Switched-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol Test Conditions

(T_J = 25°C Unless Otherwise Specified)

Characteristic Values

		Min.	Typ.	Max.
g_{fs}	I _C = 12A, V _{CE} = 10V, Note 1	6.5	10.8	S
C_{ies}	V _{CE} = 25V, V _{GE} = 0V, f = 1MHz		1290	pF
C_{oes}			56	pF
C_{res}			19	pF
Q_g	I _C = 12A, V _{GE} = 15V, V _{CE} = 1000V		62	nC
Q_{ge}			13	nC
Q_{gc}			8.5	nC
t_{d(on)}	Resistive Switching Times, T_J = 25°C I _C = 12A, V _{GE} = 15V V _{CE} = 1250V, R _G = 10Ω		64	ns
t_r			140	ns
t_{d(off)}			180	ns
t_f			540	ns
t_{d(on)}	Resistive Switching Times, T_J = 125°C I _C = 12A, V _{GE} = 15V V _{CE} = 1250V, R _G = 10Ω		65	ns
t_r			395	ns
t_{d(off)}			175	ns
t_f			530	ns
R_{thJC}	TO-247		0.21	0.78 °C/W
R_{thCS}				°C/W

Reverse Diode

Symbol Test Conditions

(T_J = 25°C Unless Otherwise Specified)

Characteristic Values

		Min.	Typ.	Max.
V_F	I _F = 12A, V _{GE} = 0V			2.1 V
t_{rr}	I _F = 6A, V _{GE} = 0V, -di _F /dt = 100A/μs		1.4	μs
I_{RM}				21 A

Note 1: Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

Littelfuse reserves the right to change limits, test conditions and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

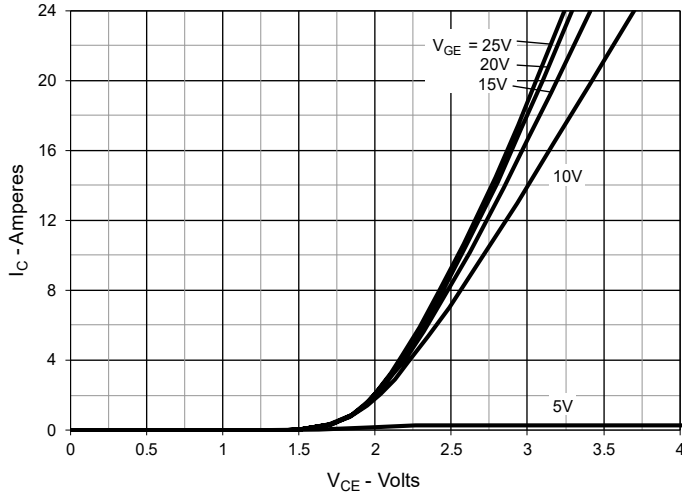


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

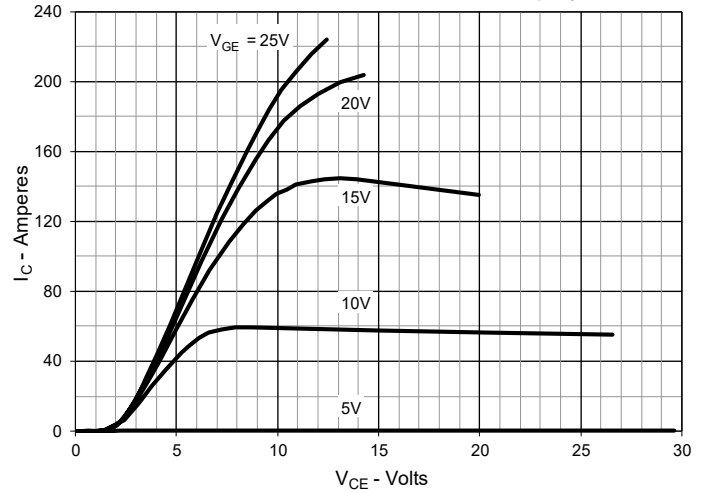


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

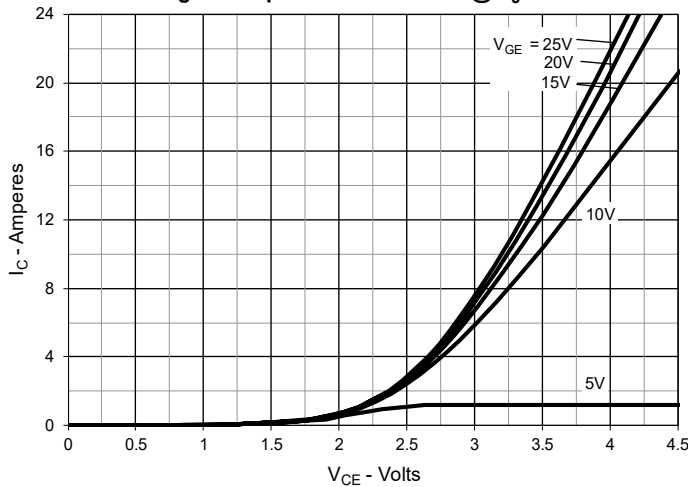


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

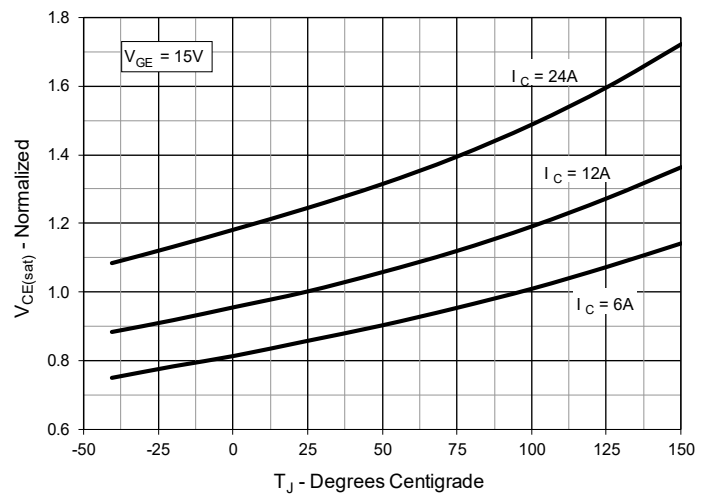


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

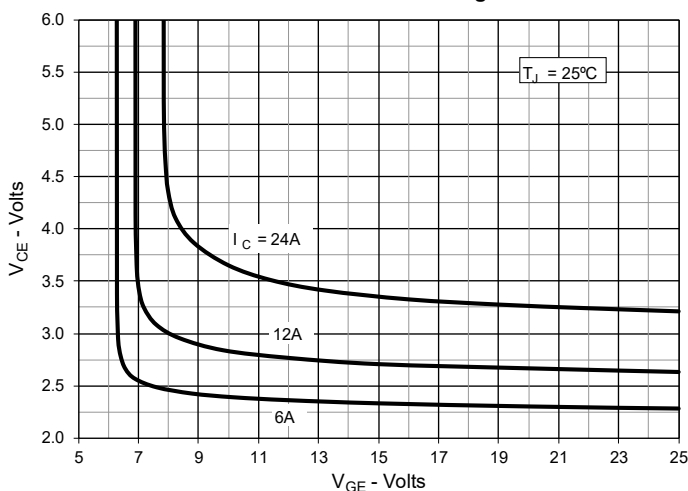


Fig. 6. Input Admittance

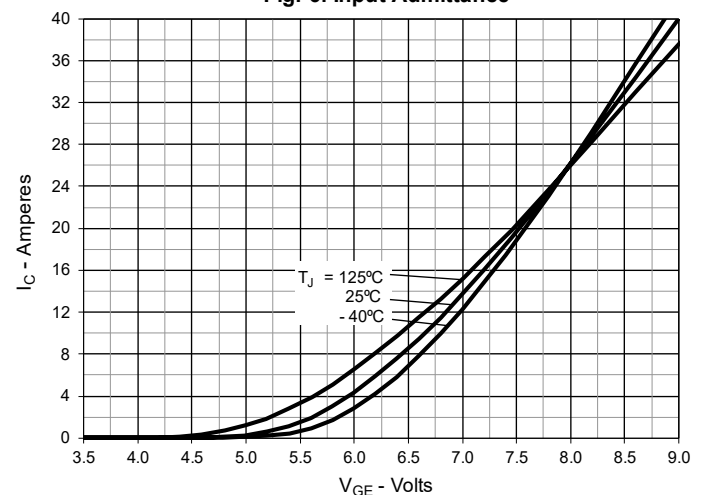


Fig. 7. Transconductance

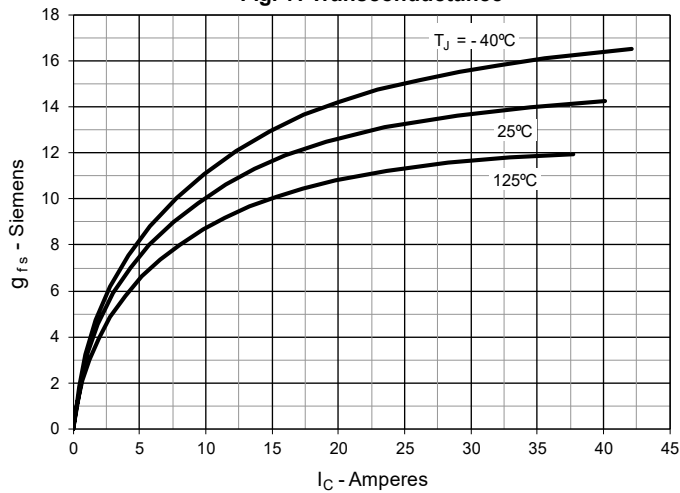


Fig. 8. Forward Voltage Drop of Intrinsic Diode

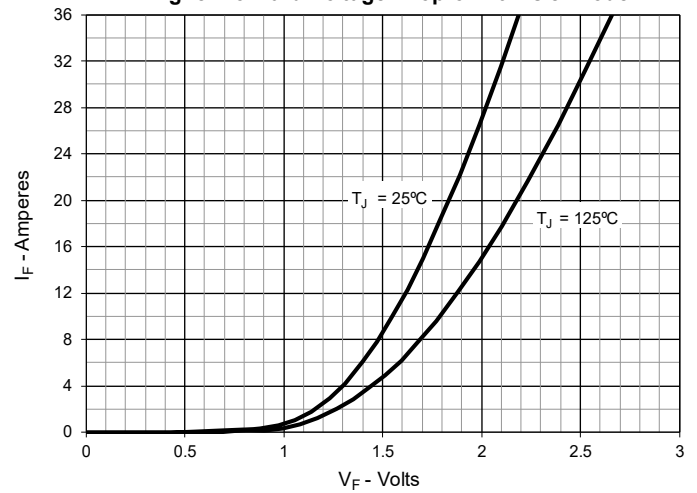


Fig. 9. Gate Charge

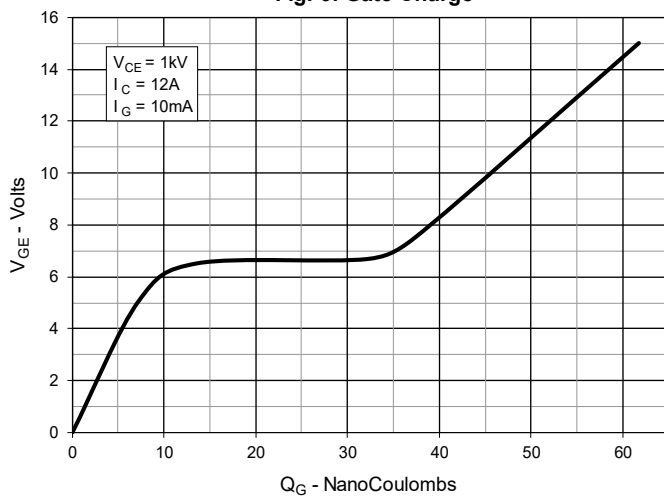


Fig. 10. Capacitance

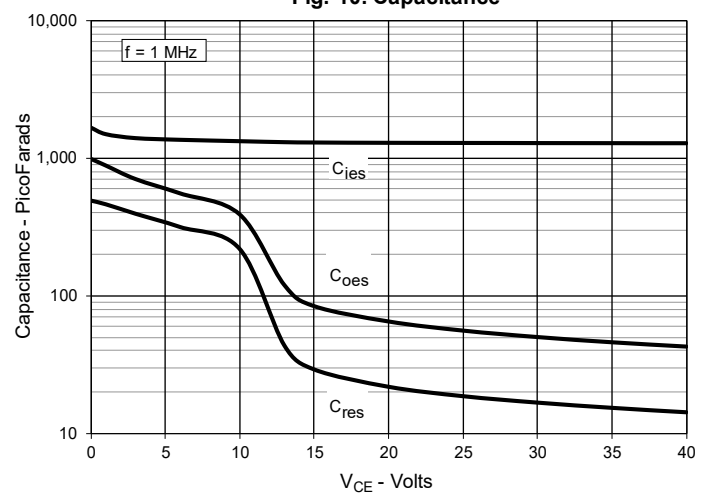


Fig. 11. Reverse-Bias Safe Operating Area

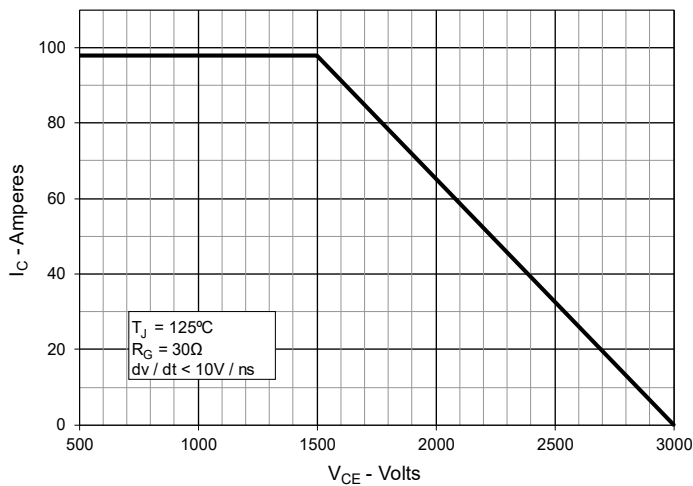


Fig. 12. Maximum Transient Thermal Impedance

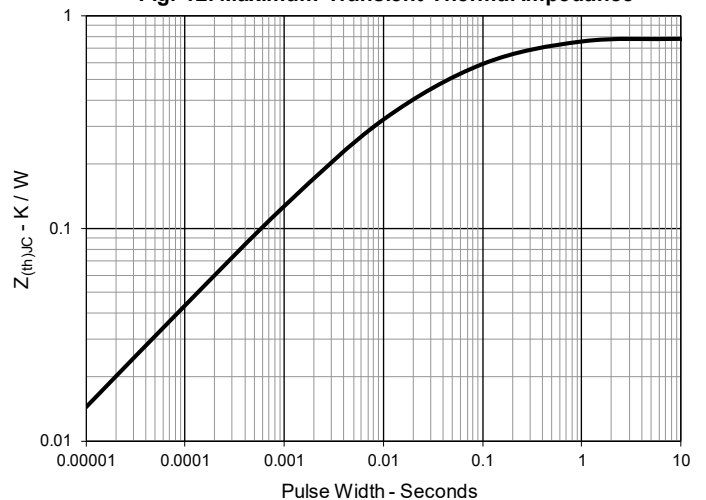


Fig. 15. Resistive Turn-on Rise Time vs. Junction Temperature

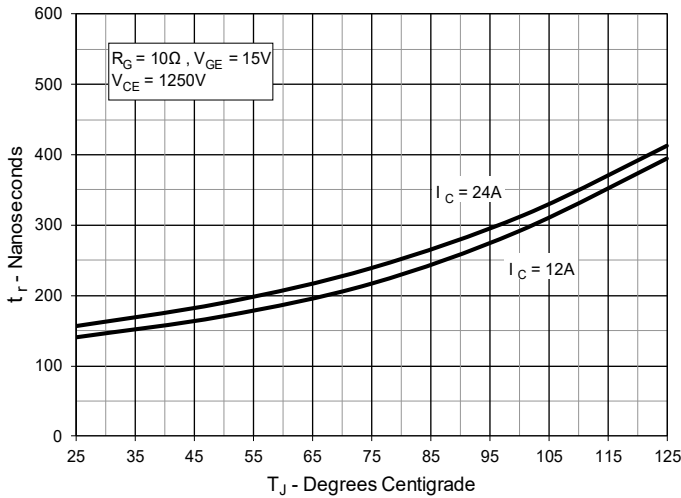


Fig. 16. Resistive Turn-on Rise Time vs. Collector Current

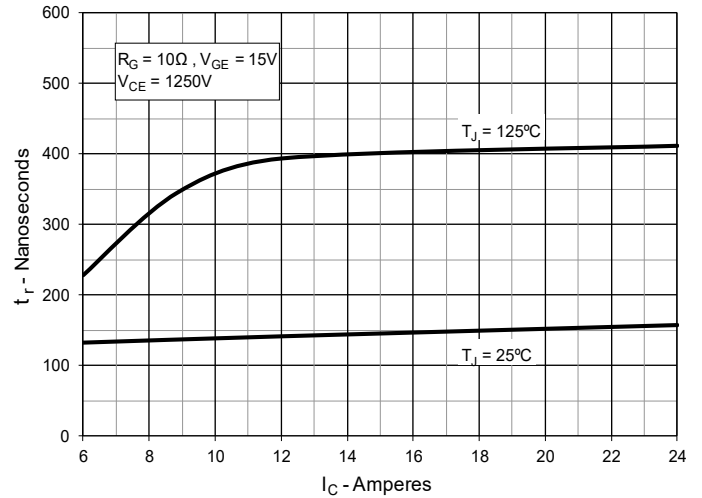


Fig. 17. Resistive Turn-on Switching Times vs. Gate Resistance

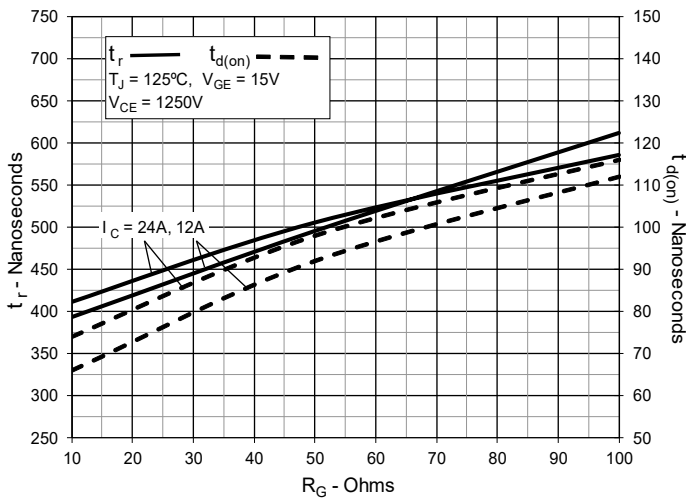


Fig. 18. Resistive Turn-off Switching Times vs. Junction Temperature

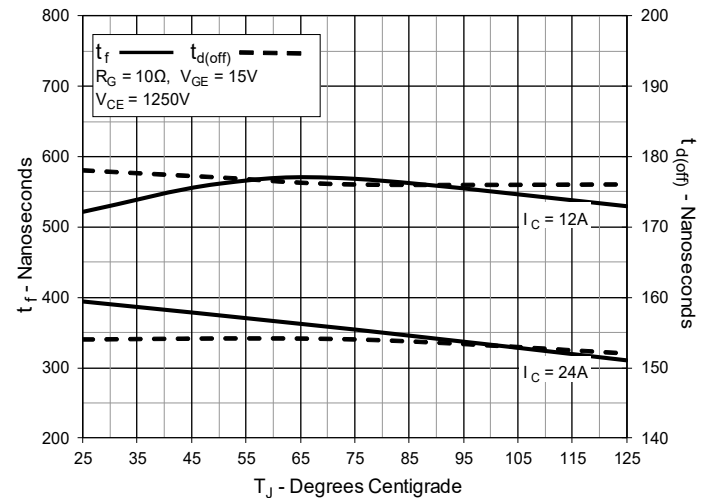


Fig. 19. Resistive Turn-off Switching Times vs. Collector Current

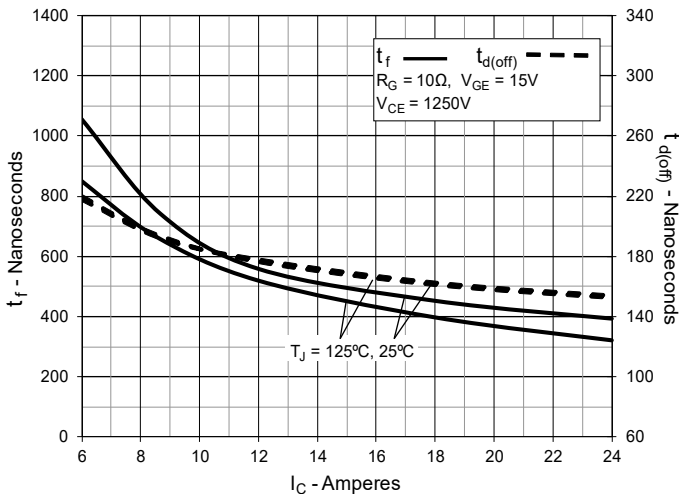
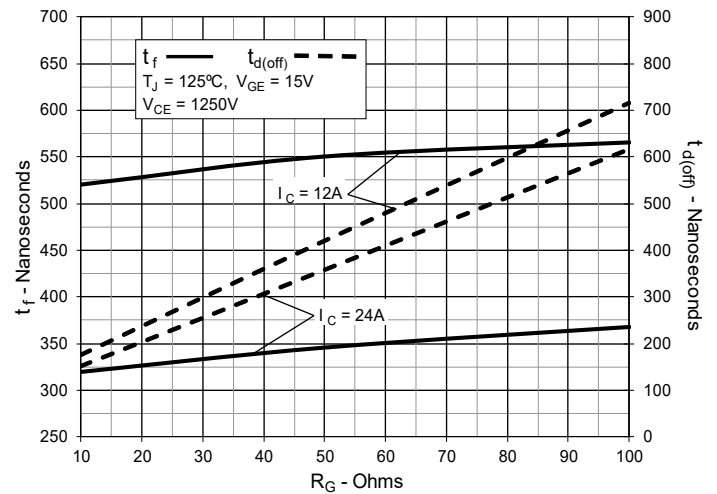
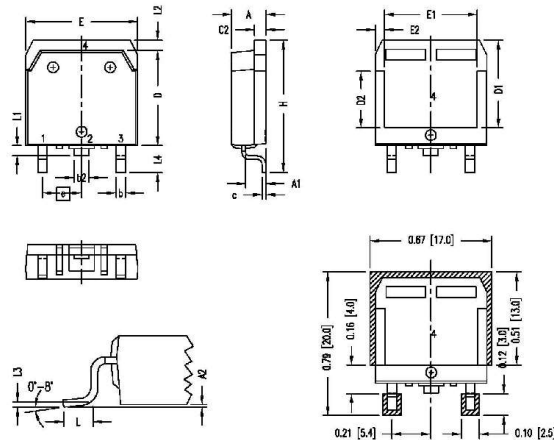


Fig. 20. Resistive Turn-off Switching Times vs. Gate Resistance



TO-268 Outline



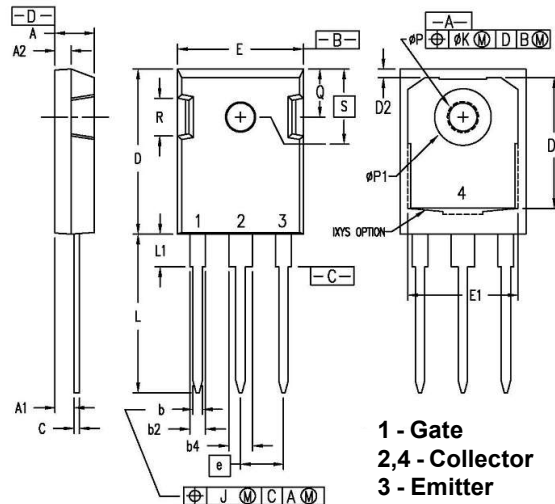
- 1 - Gate
2,4 - Collector
3 - Emitter

RECOMMENDED MINIMUM FOOT PRINT FOR SMD

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
D2	.320	.335	8.13	8.50
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
E2	.045	.055	1.14	1.39
e	.215	BSC	5.45	BSC
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010	BSC	0.25	BSC
L4	.150	.161	3.80	4.10

NOTE: ALL METAL SURFACES ARE WHITE PURE TIN PLATED EXCEPT TIRM AREA.
Pb PLATING THICKNESS (4 - 20 um)

TO-247 Outline



- 1 - Gate
2,4 - Collector
3 - Emitter

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215	BSC	5.45	BSC
J	--	.010	--	0.25
K	--	.025	--	0.64
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
øP	.140	.144	3.55	3.65
øP1	.275	.290	6.99	7.37
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242	BSC	6.15	BSC

NOTE: This drawing will meet all dimensions requirement of JEDEC outlines TO-247 AD (R-PSIP-F3)