

این دیتاشیت توسط توکل الکترونیک تهیه و ارائه شده است.
جهت مشاهده قیمت، موجودی و ثبت سفارش این قطعه به وبسایت توکل الکترونیک مراجعه فرمایید.



Rugged Power MOSFETs

File Number **2285**

IRFD9120
IRFD9123

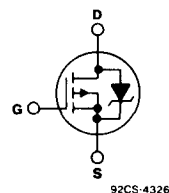
Avalanche-Energy-Rated P-Channel Power MOSFETs

-1.0 A and -0.8 A, -60 V and -100 V
 $r_{DS(on)} = 0.6 \Omega$ and 0.8Ω

Features:

- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

TERMINAL DIAGRAM

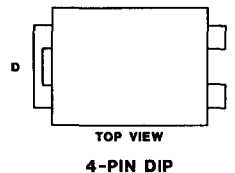


P-CHANNEL ENHANCEMENT MODE

The IRFD9120 and IRFD9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD-types are supplied in the 4-Pin dual-in-line plastic package.

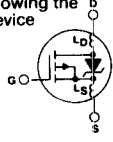
TERMINAL DESIGNATION



ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFD9120	IRFD9123	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	V
Drain-Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) ①	V_{DGR}	-100	-60	V
Continuous Drain Current	$I_D @ T_c = 25^\circ\text{C}$	-1	-0.8	A
Pulsed Drain Current ②	I_{DM}	-8	-6.4	A
Gate-Source Voltage	V_{GS}	± 20		V
Maximum Power Dissipation	$P_D @ T_c = 25^\circ\text{C}$	1.0 (See Fig. 13)		W
Linear Derating Factor		0.008 (See Fig. 13)		W/°C
Single-Pulse Avalanche Energy Rating ③	E_{as}	370		mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150		°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)		°C

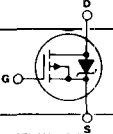
ELECTRICAL CHARACTERISTICS At Case Temperature (T_c) = 25° C Unless Otherwise Specified

CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD9120 IRFD9123	-100 -60	— —	V	$V_{GS} = 0\text{ V}$ $I_D = -250\text{ }\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$
Gate-Source Leakage Forward	I_{GSS}	ALL	—	-500	nA	$V_{GS} = -20\text{ V}$
Gate-Source Leakage Reverse	I_{SS}	ALL	—	500	nA	$V_{GS} = 20\text{ V}$
Zero-Gate Voltage Drain Current	I_{SS}	ALL	—	-250 -1000	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{ V}$ $V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{ V}$, $T_c = 125^\circ\text{C}$
On-State Drain Current ②	$I_{D(on)}$	IRFD9120 IRFD9123	-1 -0.08	— —	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\text{ max.}}$, $V_{GS} = -10\text{ V}$
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD9120 IRFD9123	— —	0.5 0.6	Ω	$V_{GS} = 10\text{ V}$, $I_D = -0.8\text{ A}$
Forward Transconductance ②	g_{fs}	ALL	0.8	1.2	S(V)	$V_{DS} \leq 50\text{ V}$, $I_D = -0.8\text{ A}$
Input Capacitance	C_{iss}	ALL	—	300	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1.0\text{ MHz}$ See Fig. 9
Output Capacitance	C_{oss}	ALL	—	200	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	pF	$V_{DD} = 0.5\text{ V}$, $I_D = -0.8\text{ A}$, $Z_o = 50\text{ }\Omega$ See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Turn-On Delay Time	$t_{d(on)}$	ALL	—	25	ns	
Rise Time	t_r	ALL	—	50	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	50	ns	
Fall Time	t_f	ALL	—	50	ns	Measured from the drain lead, 2.0mm (0.08 in.) from header to center die. Modified MOSFET symbol showing the internal device 
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	nC	
Gate-Source Charge	Q_{gs}	ALL	—	9	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	nH	
Internal Source Inductance	L_S	ALL	—	6.0	nH	Measured from the source lead, 2.0 mm (0.08 in.) from header and source bonding pad.

THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Typical socket mount
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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD9120 IRFD9123	— —	— —	-1 -0.8	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
Pulse Source Current (Body Diode)	I_{SM}	IRFD9120 IRFD9123	— —	— —	-8 -6.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD9120 IRFD9123	— —	— —	-1.5 -1.5	V	$T_c = 25^\circ\text{C}$, $I_S = -1\text{ A}$, $V_{GS} = 0\text{ V}$ $T_c = 25^\circ\text{C}$, $I_S = -0.8\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	ALL	—	150	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -4\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$
Reverse Recovered Charge	Q_{RR}	ALL	—	0.9	—	μC	$T_J = 150^\circ\text{C}$, $I_F = -4\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C .② Pulse Test: Pulse width $\leq 300\text{ }\mu\text{s}$,
Duty Cycle $\leq 2\%$.③ $V_{DD} = 25\text{ V}$, Starting $T_J = 25^\circ\text{C}$, $L = 555\text{ mH}$,
 $R_G = 25\text{ }\Omega$, Peak $I_L = 1\text{ A}$ (See Figs. 14 & 15).

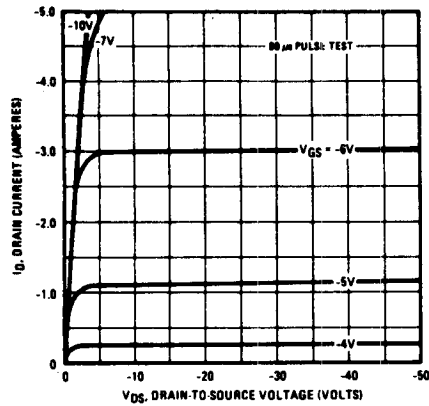


Fig. 1 - Typical output characteristics.

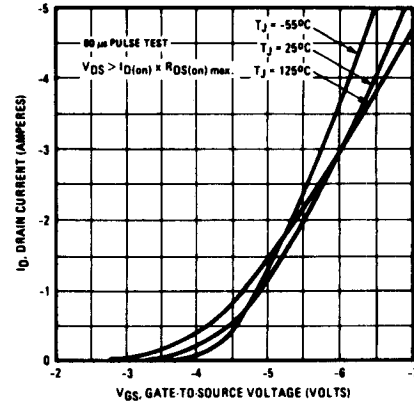


Fig. 2 - Typical transfer characteristics.

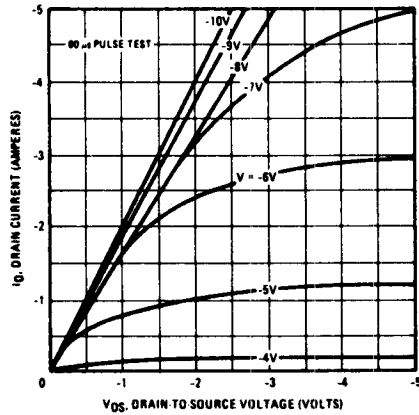


Fig. 3 - Typical saturation characteristics.

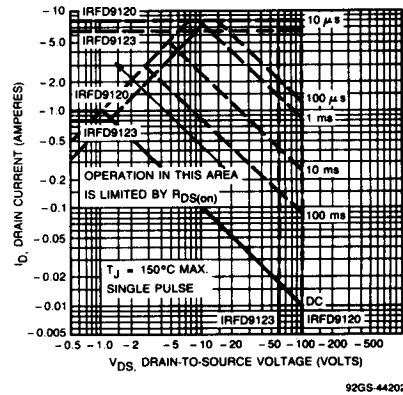


Fig. 4 - Maximum safe operating area.

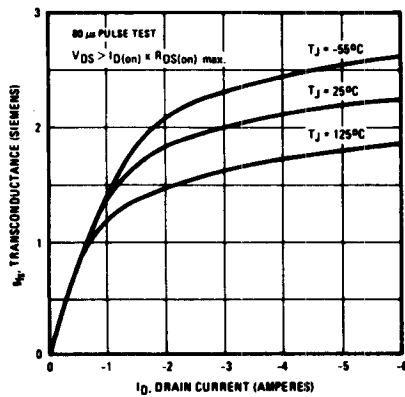


Fig. 5 - Typical transconductance vs. drain current.

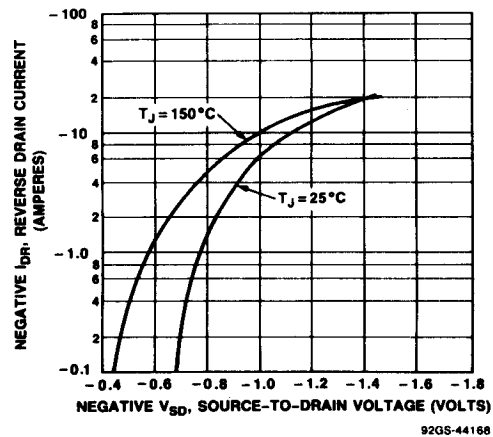


Fig. 6 - Typical source-drain diode forward voltage.

IRFD9120
IRFD9123

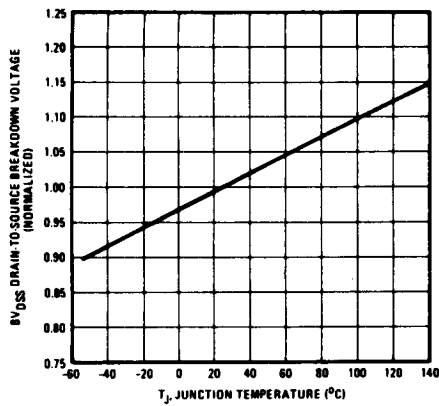


Fig. 7 - Breakdown voltage vs. temperature.

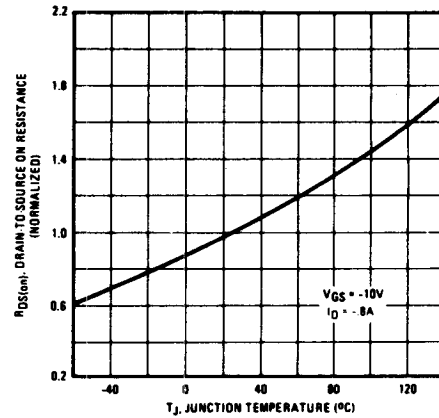


Fig. 8 - Normalized on-resistance vs. temperature.

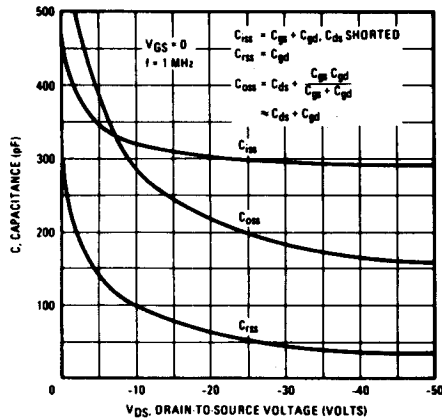


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

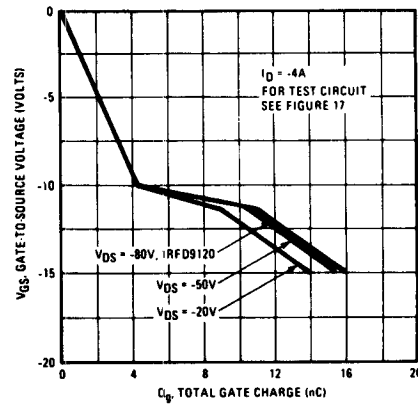


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

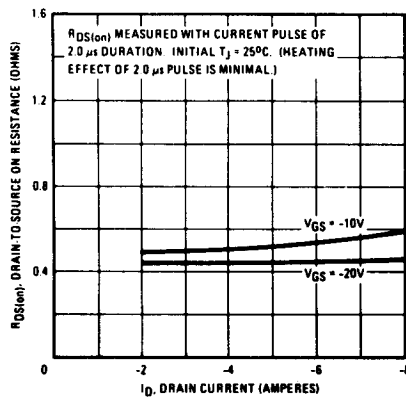


Fig. 11 - Typical on-resistance vs. drain current.

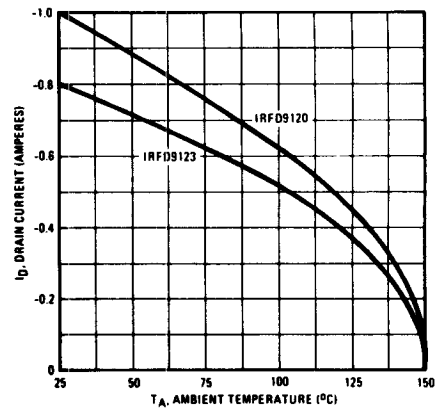


Fig. 12 - Maximum drain current vs. case temperature.

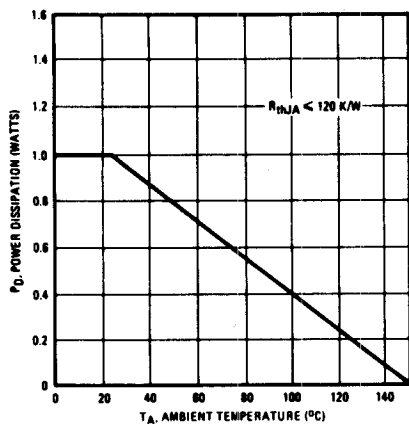


Fig. 13 - Power vs. temperature derating curve.

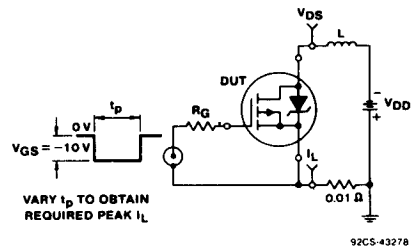


Fig. 14 - Unclamped inductive test circuit.

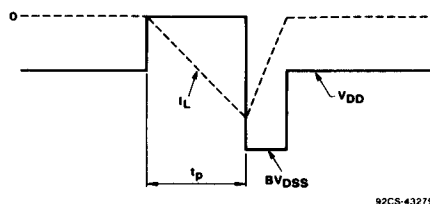


Fig. 15 - Unclamped inductive waveforms.

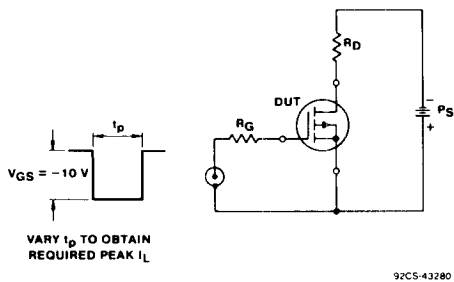


Fig. 16 - Switching time test circuit.

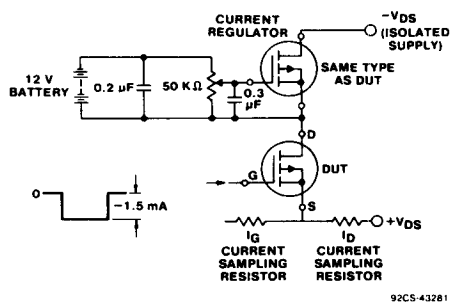


Fig. 17 - Gate charge test circuit.