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جهت مشاهده قیمت، موجودی و ثبت سفارش این قطعه به وبسایت توکل الکترونیک مراجعه فرمایید.



مشاهده قیمت و خرید
برای خرید و مشاهده سایر محصولات کلیک کنید

FAIRCHILD
SEMICONDUCTOR

October 2001

FDS4435

FDS4435

30V P-Channel PowerTrench[®] MOSFET

General Description

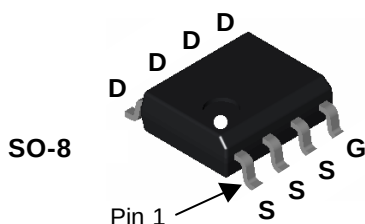
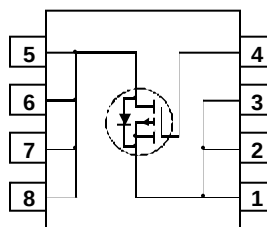
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 25V).

Applications

- Power management
- Load switch
- Battery protection

Features

- –8.8 A, –30 V $R_{DS(ON)} = 20\text{ m}\Omega$ @ $V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 35\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$
- Low gate charge (17nC typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	–30	V
V_{GSS}	Gate-Source Voltage	± 25	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	–8.8	A
		–50	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.5	W
		1.2	
		1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Package Marking and Ordering Information

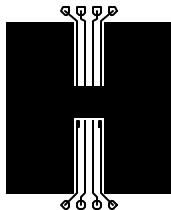
Device Marking	Device	Reel Size	Tape width	Quantity
FDS4435	FDS4435	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

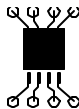
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = -250\text{ }\mu\text{A}$	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_b = -250\text{ }\mu\text{A}$, Referenced to 25°C		–21		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = -250\text{ }\mu\text{A}$	–1	–1.7	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_b = -250\text{ }\mu\text{A}$, Referenced to 25°C		5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_b = -8.8\text{ A}$ $V_{GS} = -4.5\text{ V}, I_b = -6.7\text{ A}$ $V_{GS} = -10\text{ V}, I_b = -8.8\text{ A}, T_J = 125^\circ\text{C}$		15 22 19	20 35 32	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	–50			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_b = -8.8\text{ A}$		24		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$		1604		pF
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$		408		pF
C_{rss}	Reverse Transfer Capacitance			202		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_b = -1\text{ A},$		13	23	ns
t_r	Turn–On Rise Time	$V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		13.5	24	ns
$t_{d(off)}$	Turn–Off Delay Time			42	68	ns
t_f	Turn–Off Fall Time			25	40	ns
Q_g	Total Gate Charge	$V_{DS} = -15\text{ V}, I_b = -8.8\text{ A},$		17	24	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -5\text{ V}$		5		nC
Q_{gd}	Gate–Drain Charge			6		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)		–0.73	–1.2	V

Notes:

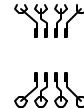
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 105°C/W when mounted on a $.04\text{ in}^2$ pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

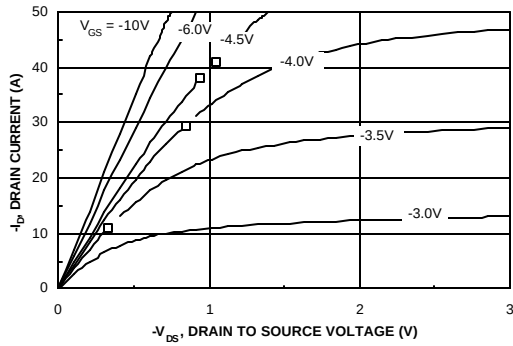


Figure 1. On-Region Characteristics.

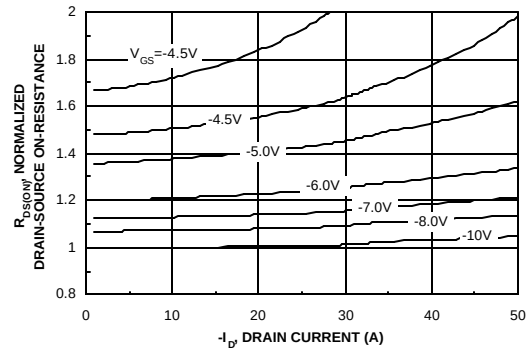


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

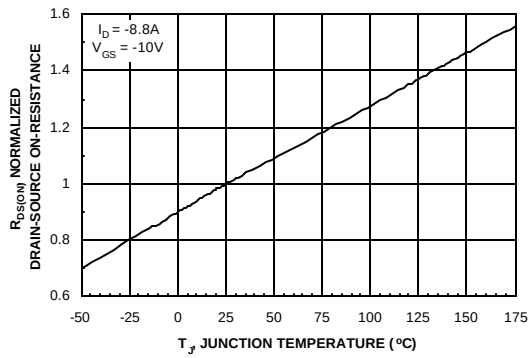


Figure 3. On-Resistance Variation with Temperature.

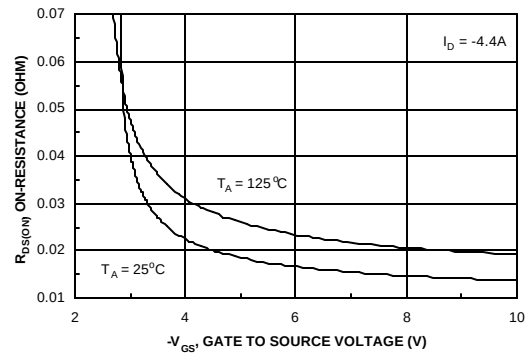


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

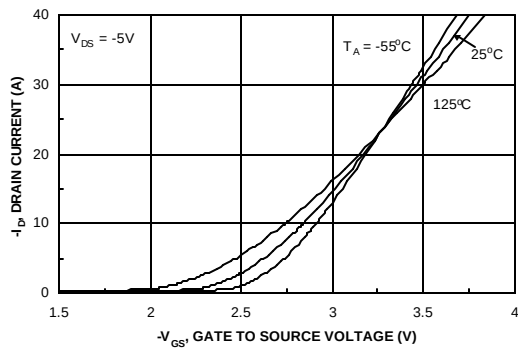


Figure 5. Transfer Characteristics.

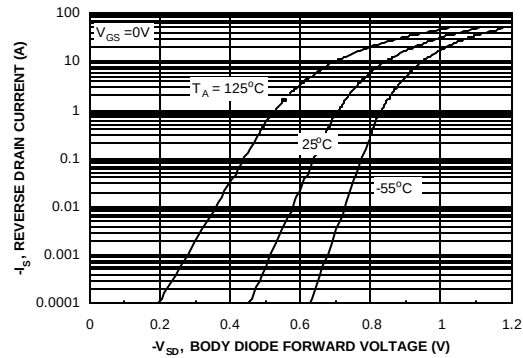


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

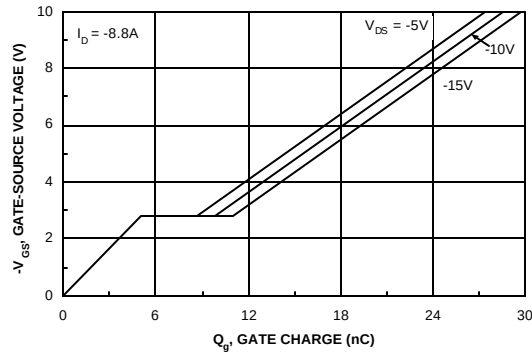


Figure 7. Gate Charge Characteristics.

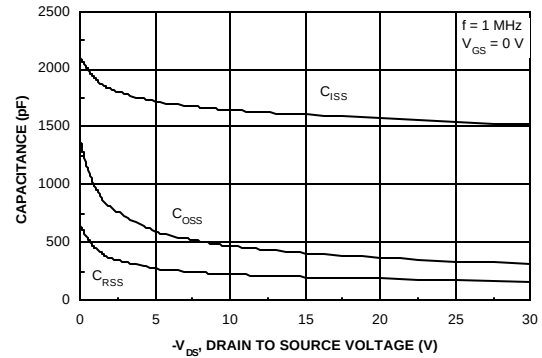


Figure 8. Capacitance Characteristics.

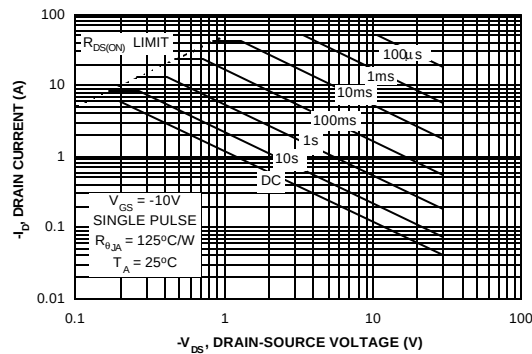


Figure 9. Maximum Safe Operating Area.

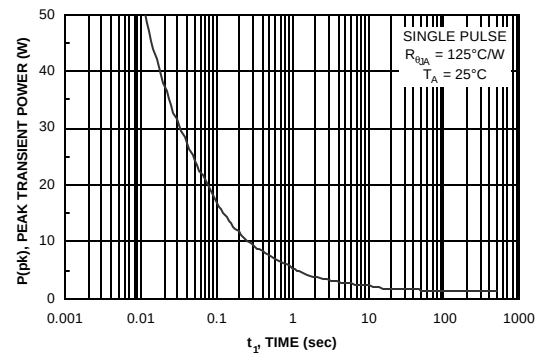


Figure 10. Single Pulse Maximum Power Dissipation.

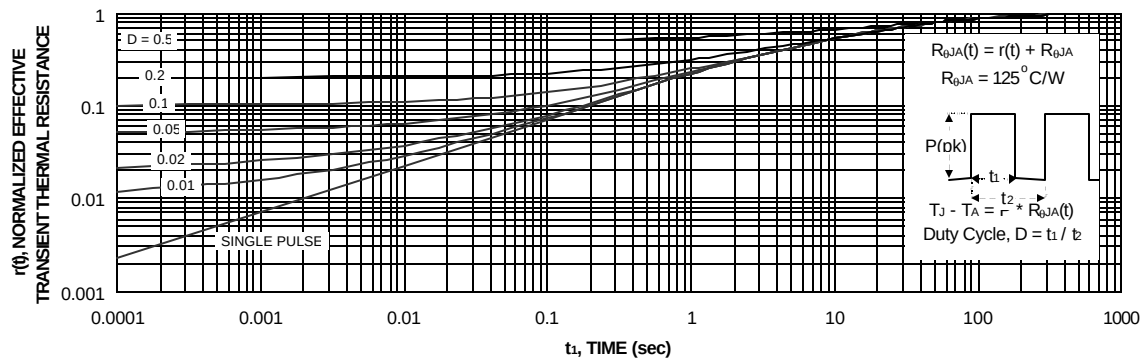


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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